What is claimed is:

1. A semiconductor memory device comprising:

a memory cell array which includes a plurality of memory cells;

a bitline and a complementary bitline which are connected to the memory cell array;

a coupling capacitor one end of which is connected to either the bitline or the complementary bitline and the other end of which a control signal is applied to;

a bitline sensing amplifier which senses and amplifies a difference in the voltage between the bitline and the complementary bitline; and

a control circuit which generate the control signal,

wherein an internal power supply generated by dropping an external power supply applied from the outside of the semiconductor memory device is used as a power supply of the control circuit.

2. The semiconductor memory device of claim 1, wherein the internal power supply determines a 'high' active restoration level in restoring the bitline.

3. The semiconductor memory device of claim 1, wherein the control circuit comprises an inverter, which outputs the control signal, the internal power supply is applied to a source of a PMOS transistor of the inverter, and the external power supply is applied to a bulk of the PMOS transistor of the inverter.

4. The semiconductor memory device of claim 1, wherein the control circuit comprises an inverter, which outputs the control signal, and the internal power supply is applied to a source and a bulk of a PMOS transistor of the inverter.

5. The semiconductor memory device of claim 1, wherein the internal power supply is used as a power supply of the bitline sensing amplifier.

6. A semiconductor memory device comprising:

a memory cell array which includes a plurality of memory cells;

a bitline and a complementary bitline which are connected to the memory cell array;

a coupling capacitor one end of which is connected to either the bitline or the complementary bitline and the other end of which a control signal is applied to;

a bitline sensing amplifier which senses and amplifies a difference in the voltage between the bitline and the complementary bitline;

a switch circuit which varies a power supply of the control circuit in response to a plurality of power control signals; and

a mode register set which generates the power control signals in response to a command applied from the outside of the semiconductor memory device.

7. The semiconductor memory device of claim 6, wherein the switch circuit comprises:

a first switch which provides a boosted voltage generated by boosting an external power supply applied from the outside as a power supply of the control circuit in response to activation of a first power control signal;

a second switch which provides the external power supply as the power supply of the control circuit in response to activation of a second power control signal;

a third switch which provides an internal power supply generated by dropping the external power supply as the power supply of the control circuit in response to activation of a third power control signal; and

a fourth switch which provides another internal power supply generated by dropping the external power supply as the power supply of the control circuit in response to activation of a fourth power control signal.

8. The semiconductor memory device of claim 6, wherein the control circuit comprises an inverter, which outputs the control signal, and an output signal of the switch circuit is applied to a source and a bulk of a PMOS transistor of the inverter.